Amendments to the Claims

The following listing of the claims will replace all prior versions, and listings of the claims in the application:

Listing of Claims

1. (Currently amended) An apparatus for reproducing information that has been digitally recorded on a storage medium, the apparatus comprising:

a first waveform equalizer which equalizes a read signal corresponding to the information read out from the storage medium, thereby outputting a first equalized signal; and

a second waveform equalizer, which has an equalization characteristic different from an equalization characteristic ~~that~~ of the first waveform equalizer, outputs a second equalized signal and is selectively used to extract a read clock signal for application to a phase locked loop, wherein the second waveform equalizer has an equalization characteristic which emphasizes high frequency components of the input signal more strongly than does the equalization characteristic of the first waveform equalizer.

2-3 Canceled

4. (Original) The apparatus of claim 1, further comprising:

a clock generator for outputting the read clock signal responsive to the second equalized signal; and

a decoder for generating digitized data from the first equalized signal.

5. (Original) The apparatus of claim 4, further comprising:

a phase shifter for shifting, responsive to a phase control signal, the phase of the read clock signal that has been output from the clock generator and outputting a phase shifted read clock signal as a sampling clock signal;

an A/D converter for converting the first equalized signal into a digital read signal by sampling the first equalized signal by reference to the sampling clock signal that has been output from the phase shifter; and

a phase control signal generator for detecting a phase deviation of the sampling clock signal in accordance with the digital read signal that has been output from the A/D converter and outputting the phase control signal to the phase shifter so as to reduce the phase deviation of the sampling clock signal, wherein the decoder generates the digitized data from the digital read signal that has been output from the A/D converter.

6. (Original) The apparatus of claim 4, wherein the decoder performs its decoding operation in accordance with a pattern of a digital read signal that has been obtained by sampling the first equalized signal.

7. (Currently amended) The apparatus of claim 6, wherein the decoder operates in accordance with a partial response maximum likelihood ~~PRML~~ method.

8. (Original) The apparatus of claim 1, wherein the storage medium is an optical disk.

9. (New) The apparatus of claim 1, wherein the first waveform equalizer has an equalization level which is smaller than an equalization level of the second waveform equalizer.

10. (New) The apparatus of claim 1, further including a first equalization characteristic controller, wherein the first equalization characteristic controller receives a signal to be input to a maximum likelihood detector and a signal output from the maximum likelihood detector and performs feedback control over the equalization characteristic of the first waveform equalizer.

11. (New) The apparatus of claim 1, further including a second equalization characteristic controller, wherein the second equalization characteristic controller receives the read clock signal and performs feedback control over the equalization characteristic of the second waveform equalizer.